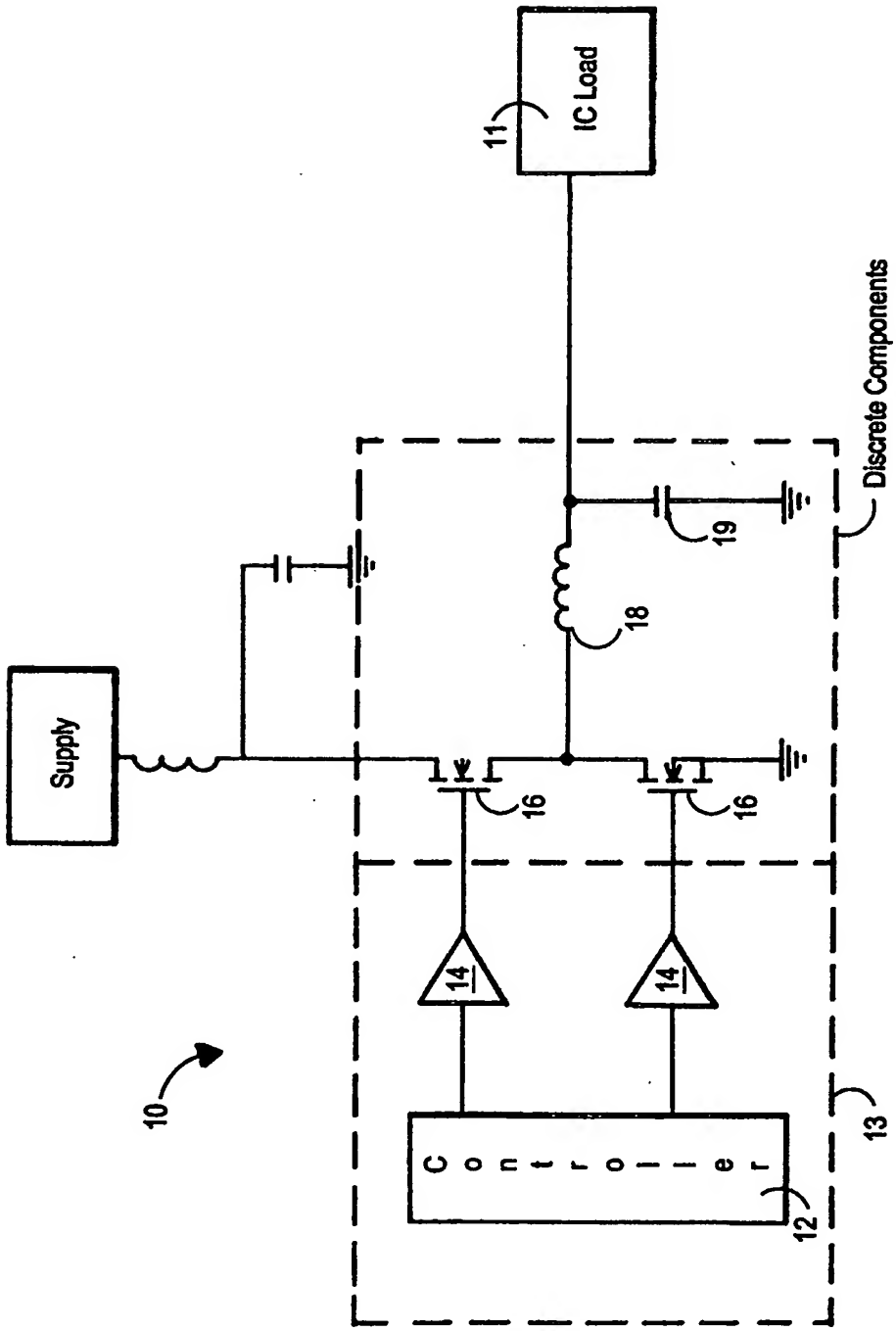


FIG. 1 - PRIOR ART

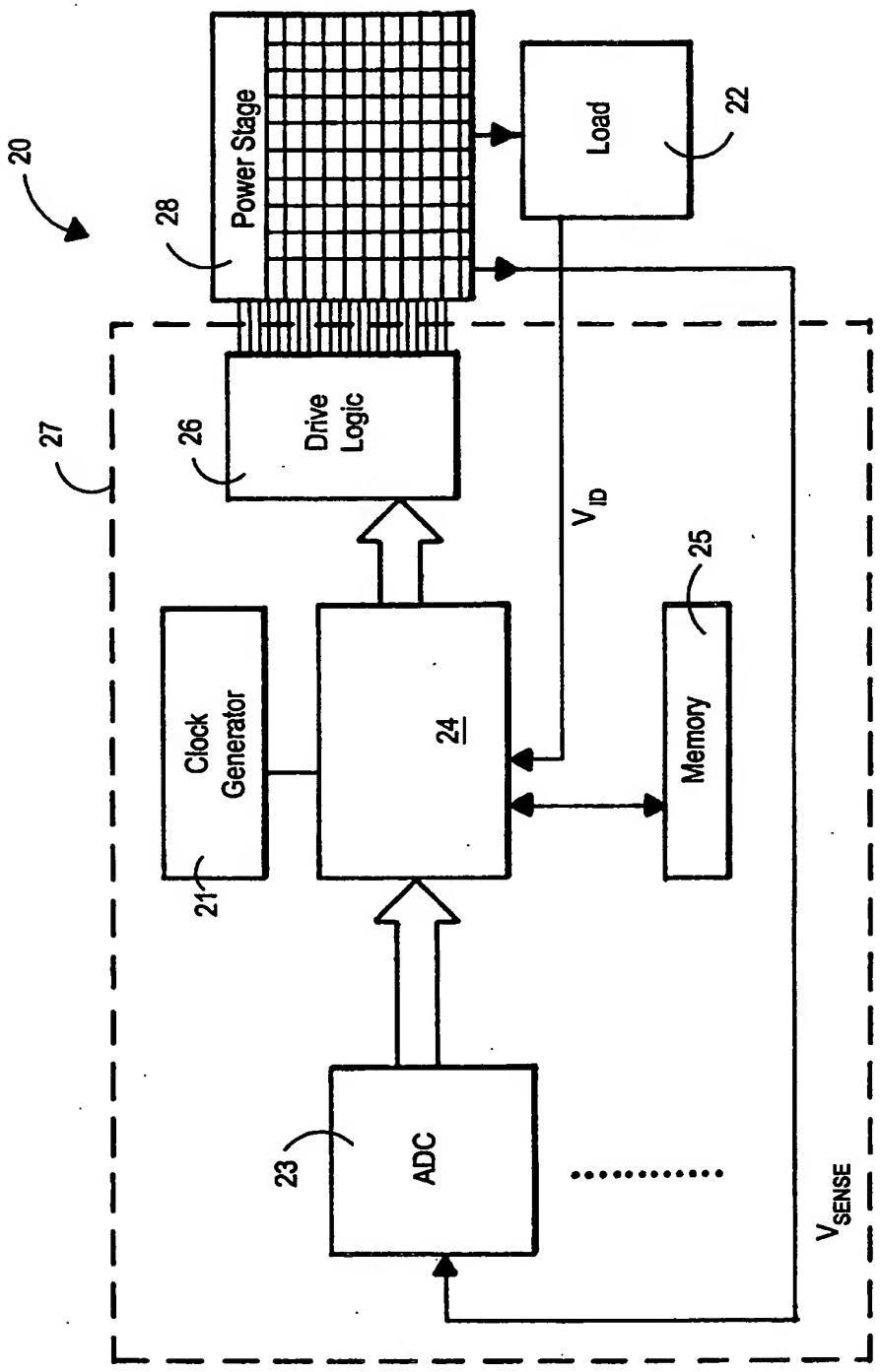


FIG. 2

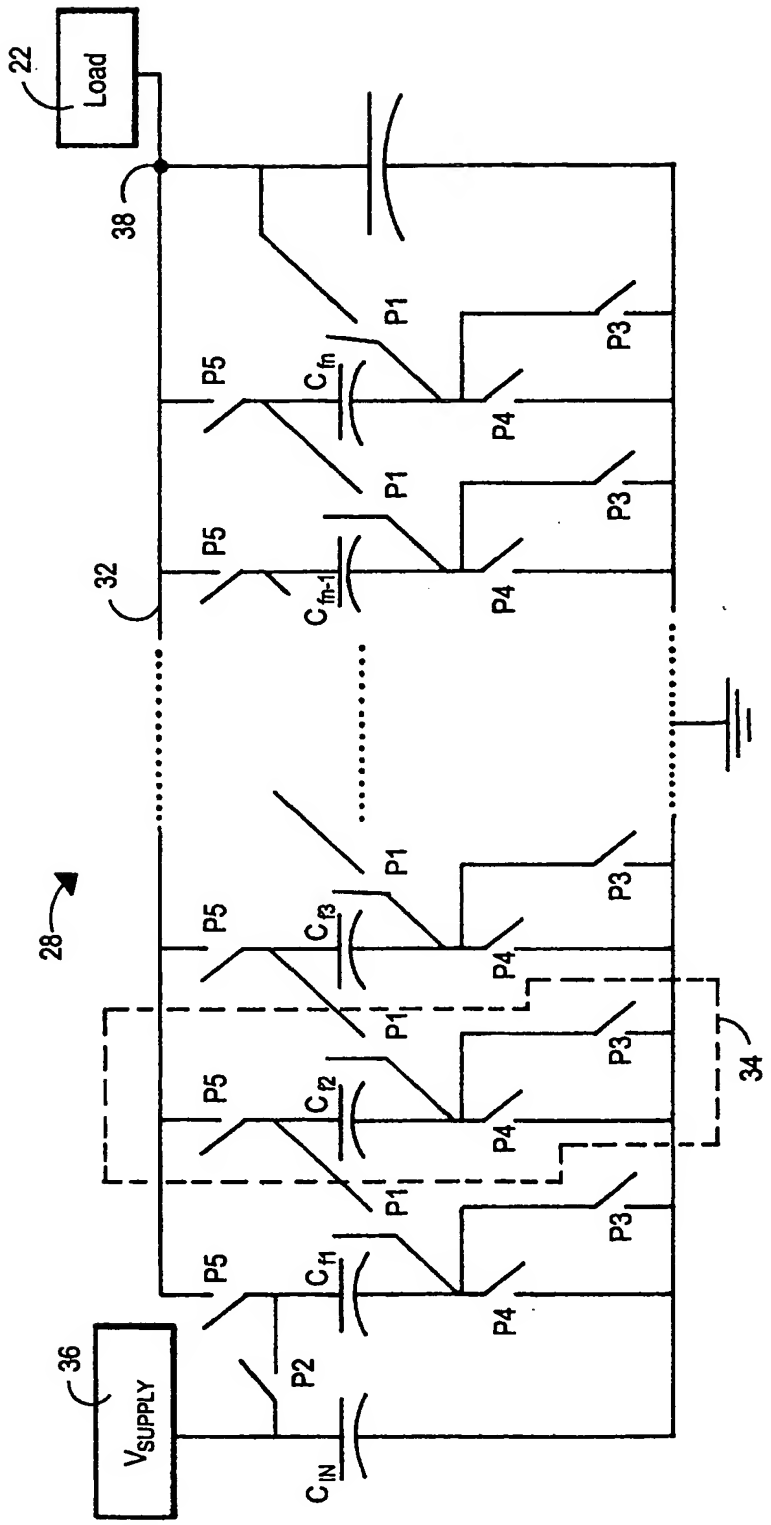

22
Load
38
32
28
36
V_{SUPPLY}
C_{IN}
C_{f1}
C_{f2}
C_{f3}
C_{fn-1}
C_{fn}
P1
P2
P3
P4
P5
34

FIG. 3

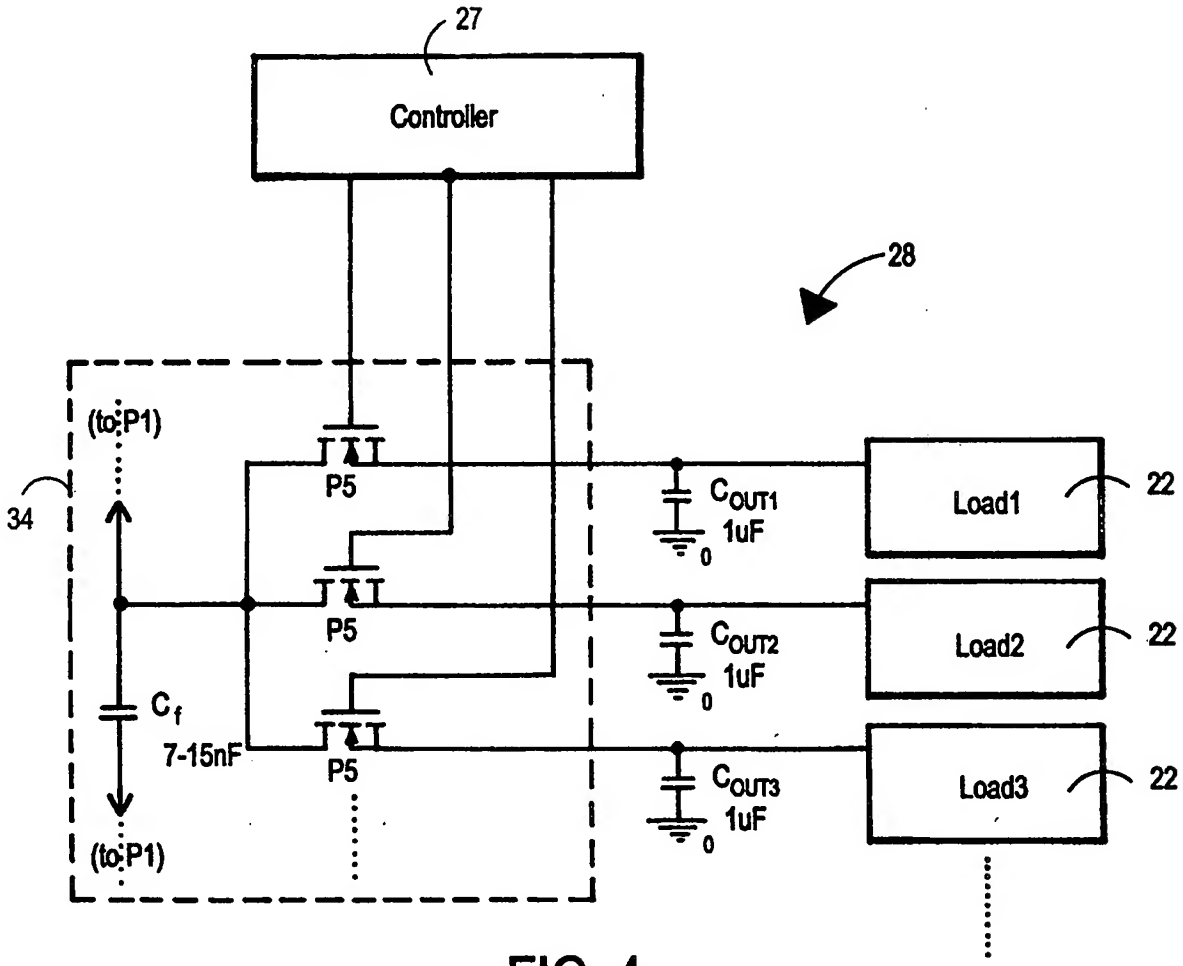

27
Controller
28
(to P1)
34
P5
P5
P5
C_f
7-15nF
(to P1)
C_{OUT1}
1uF
C_{OUT2}
1uF
C_{OUT3}
1uF
Load1
Load2
Load3
22
22
22

FIG. 4

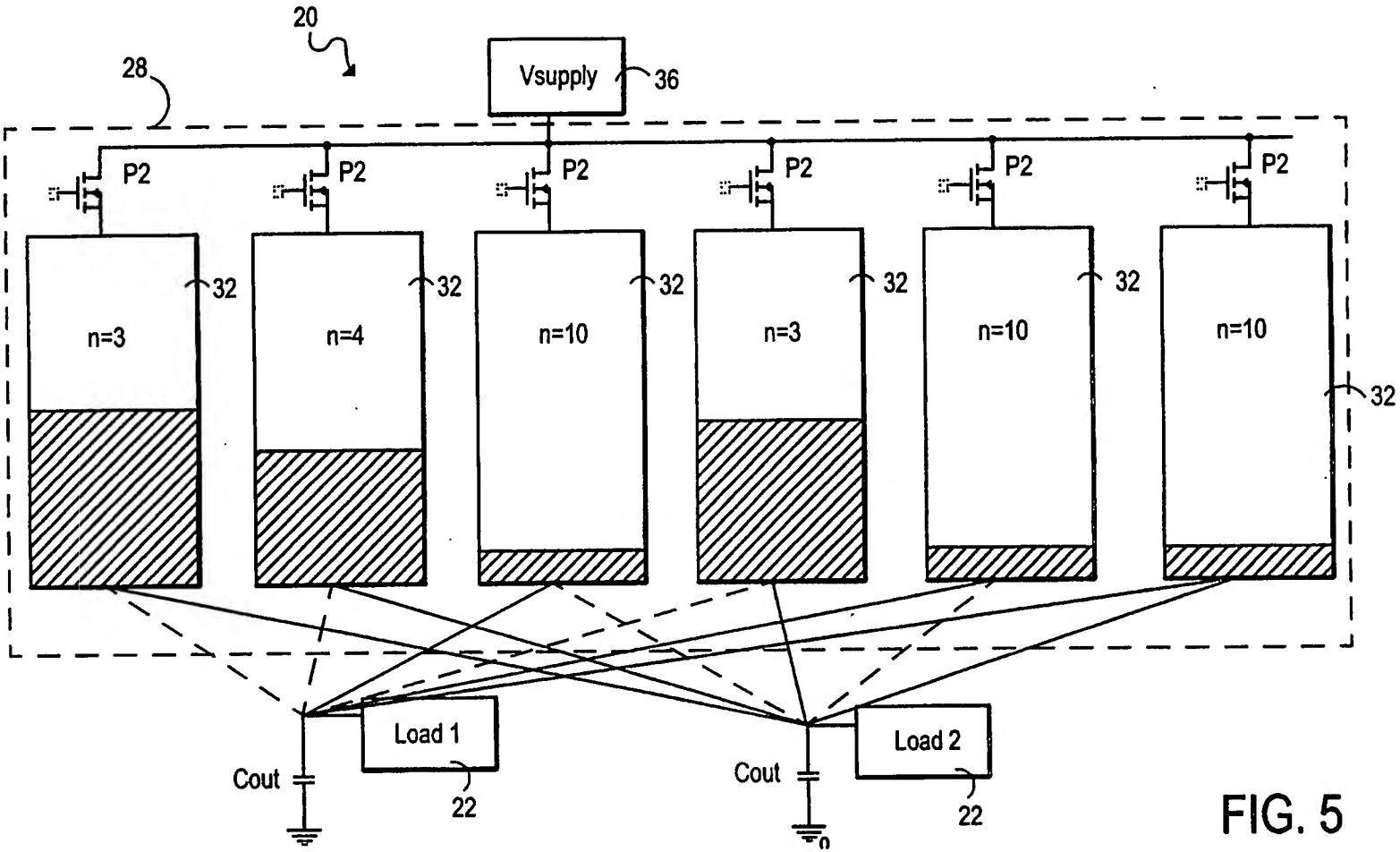

20
28
Vsupply
36
P2
P2
P2
P2
P2
P2
32
32
32
32
32
32
32
n=3
n=4
n=10
n=3
n=10
n=10
Load 1
Load 2
Cout
Cout
22
22

FIG. 5

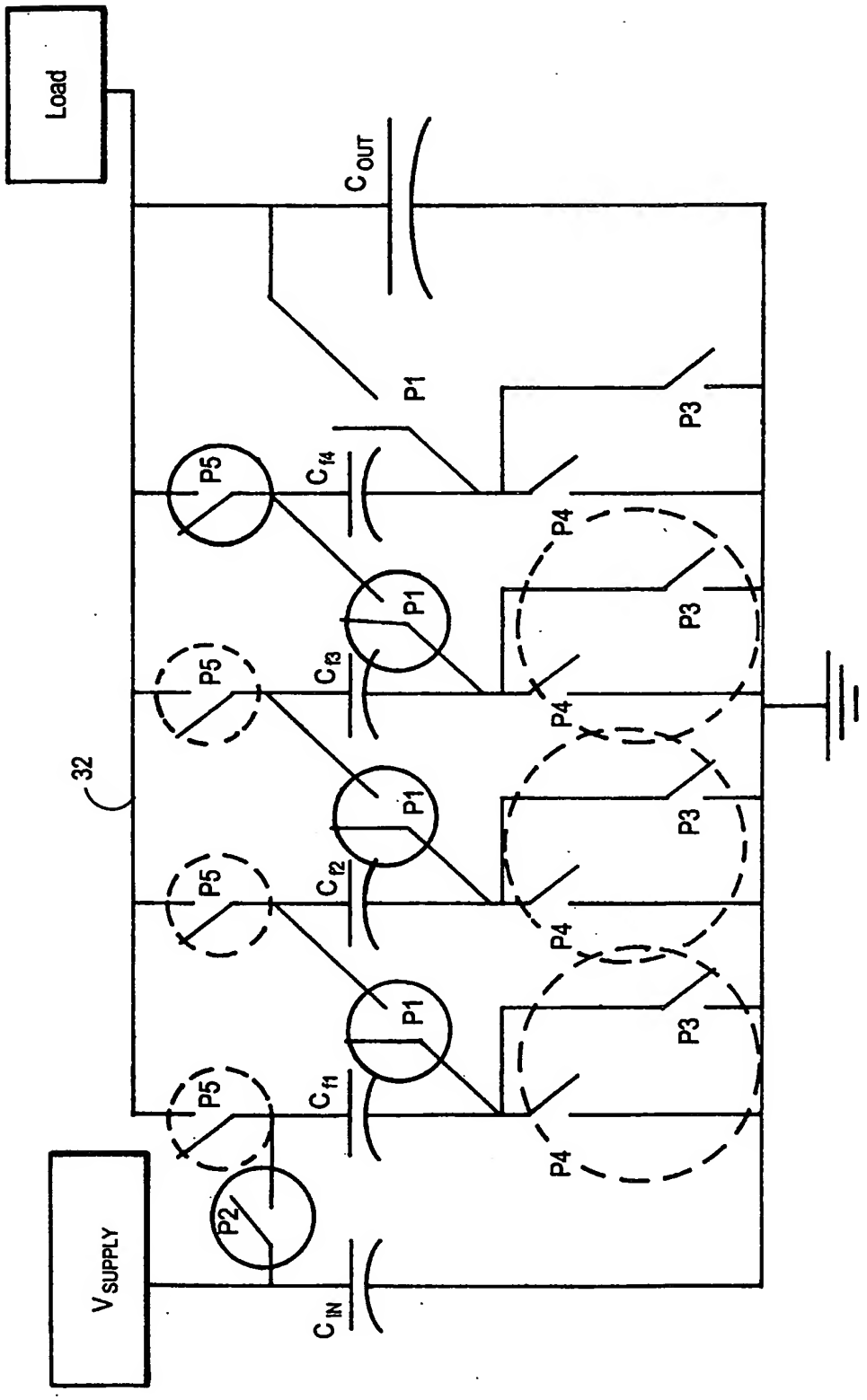

Load
C_{OUT}
P1
P3
P5
C_{f4}
P4
P1
P3
P5
C_{f3}
P4
32
P1
P3
P5
C_{f2}
P4
P1
P3
P5
C_{f1}
P4
P2
V_{SUPPLY}
C_{IN}

FIG. 6

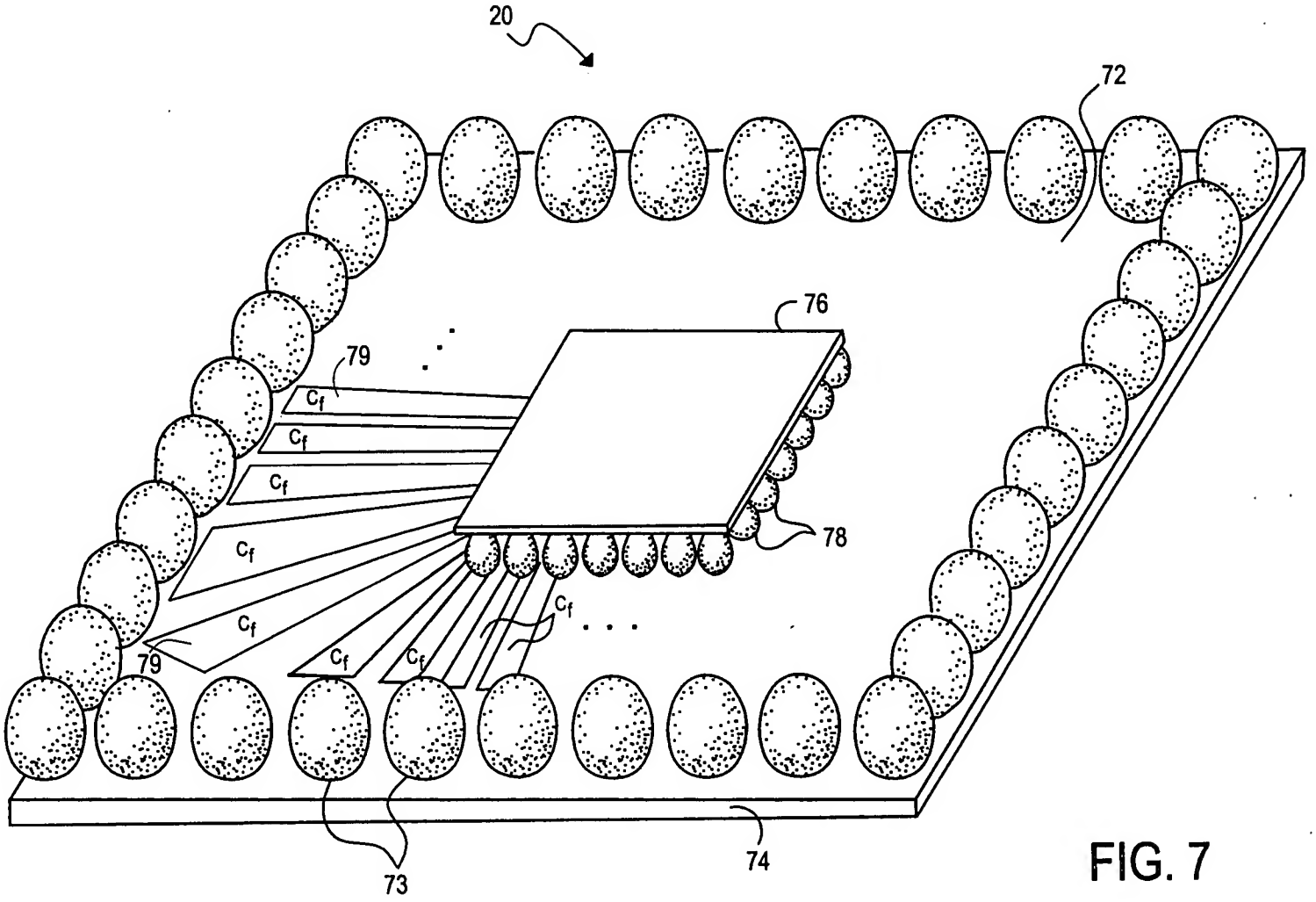


FIG. 7

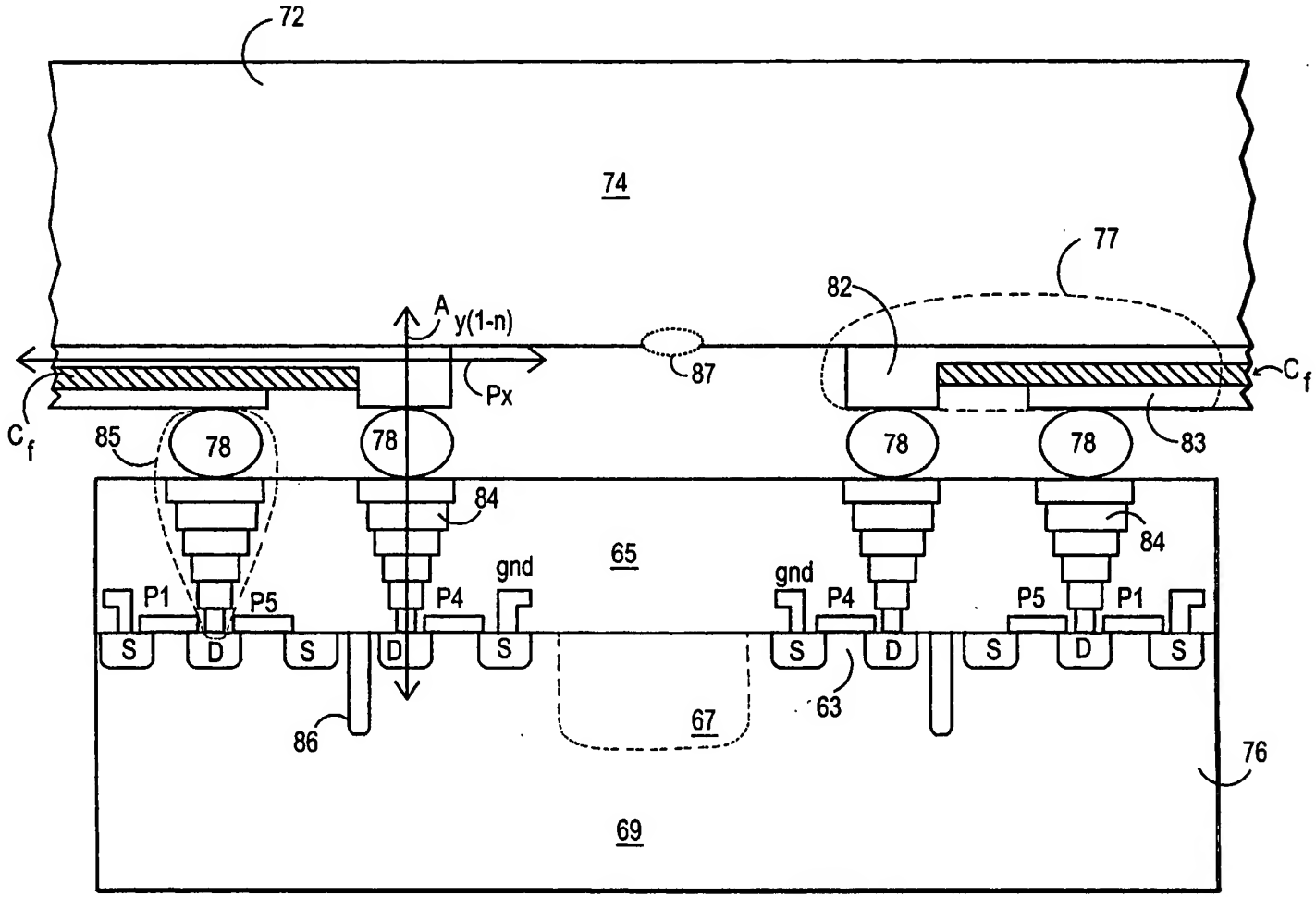

72
74
77
82
A
y(1-n)
87
Px
C_f
C_f
85
78
78
78
78
83
84
84
65
gnd
gnd
P1
P5
P4
P4
P5
P1
S
D
S
D
S
S
D
S
D
S
86
67
63
76
69

FIG. 8

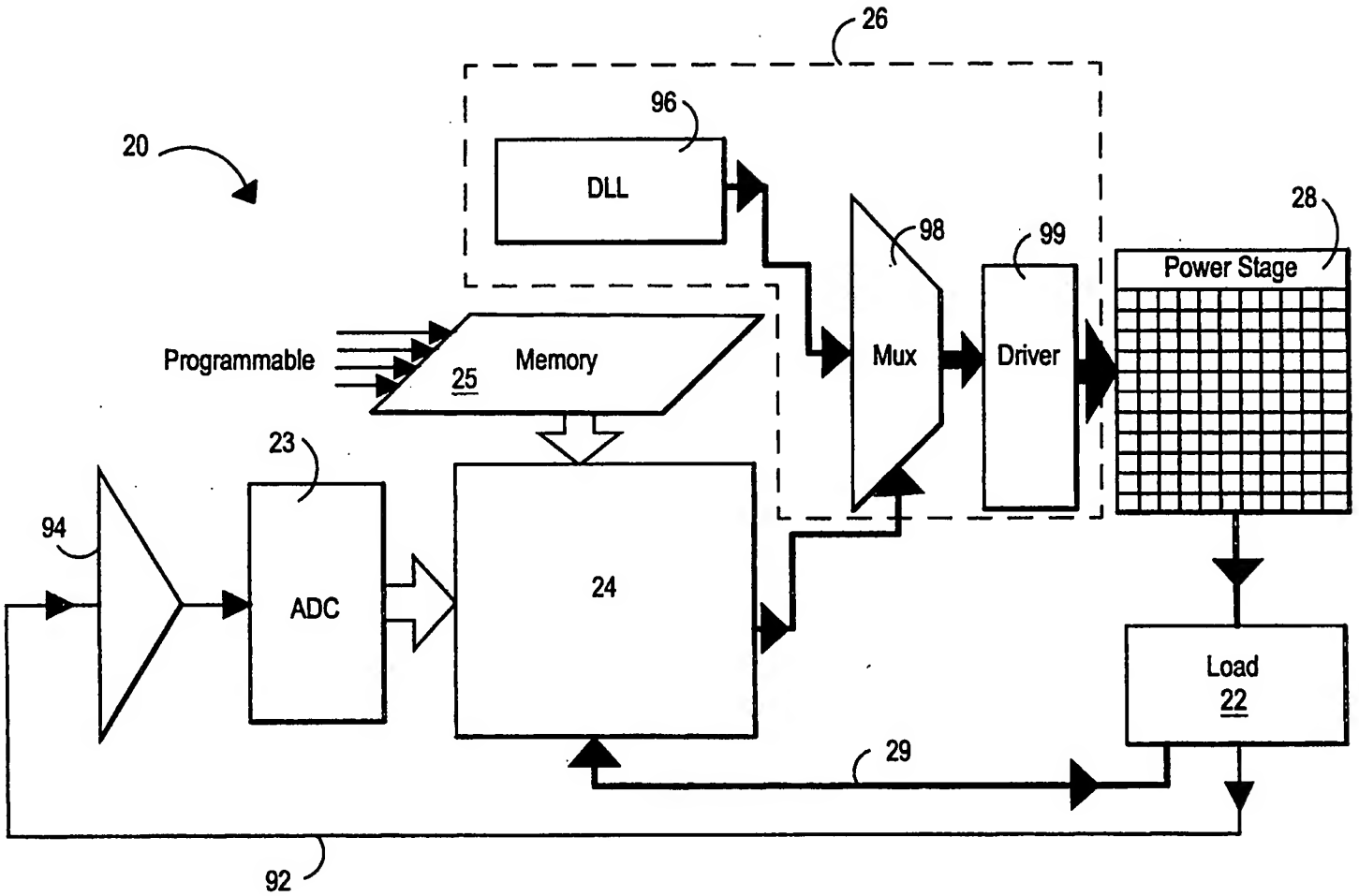

26
96
20
DLL
28
98
99
Power Stage
Programmable
Memory
25
Mux
Driver
23
94
ADC
24
Load
22
29
92

FIG. 9

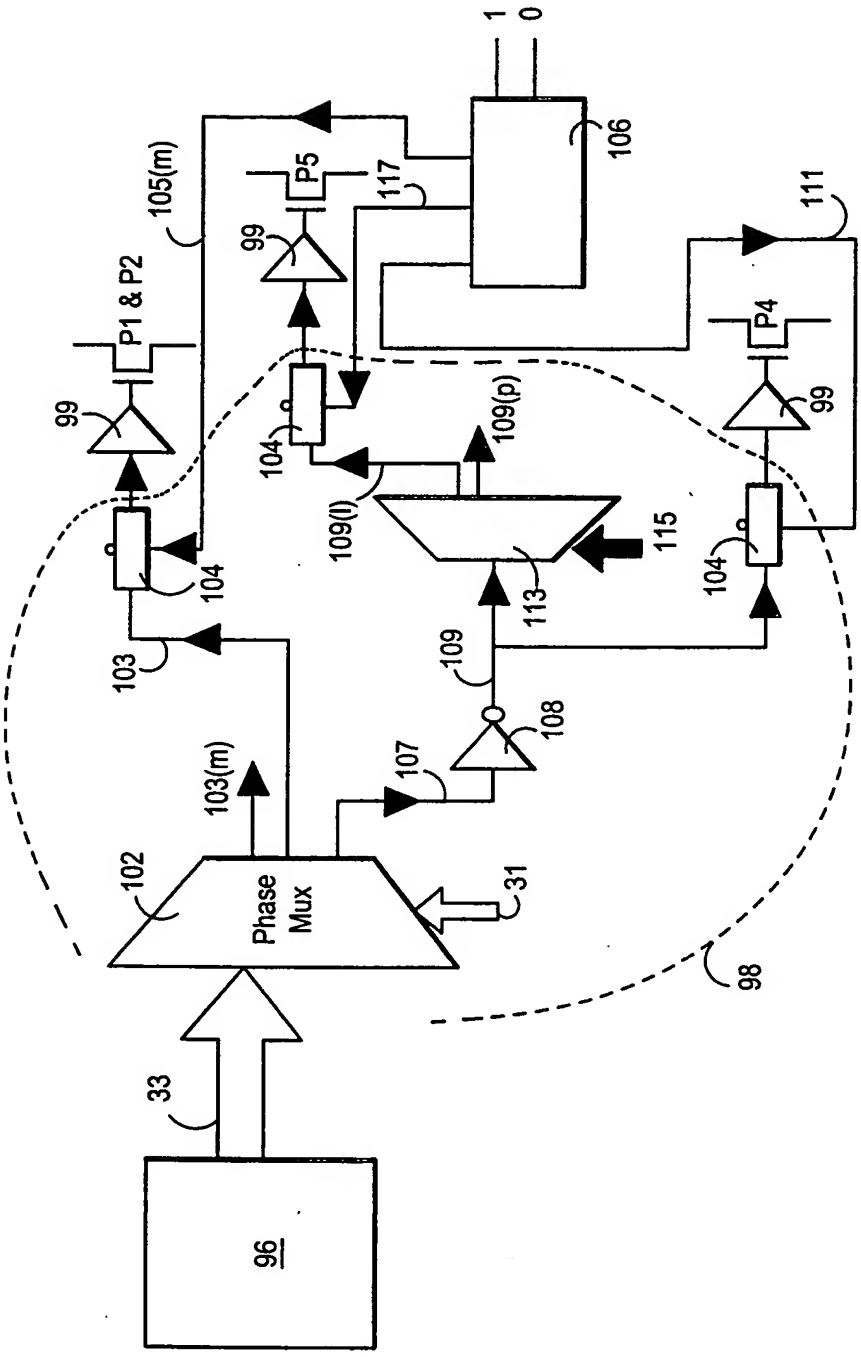

96
33
Phase Mux
102
103(m)
103
104
105(m)
106
107
108
109
109(l)
109(p)
111
113
115
117
31
98
99
P1 & P2
P4
P5
1
0

FIG. 10

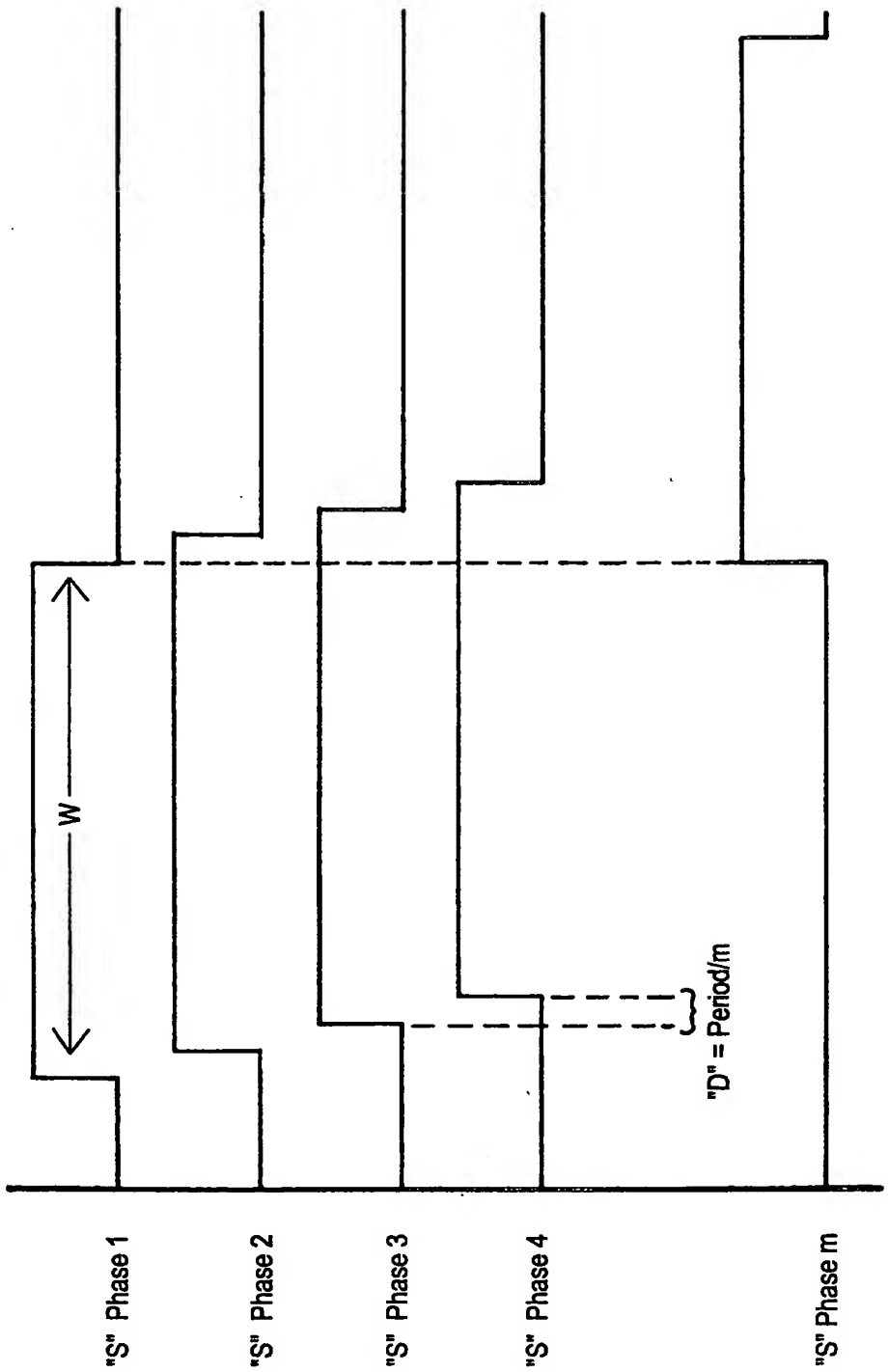


FIG. 11

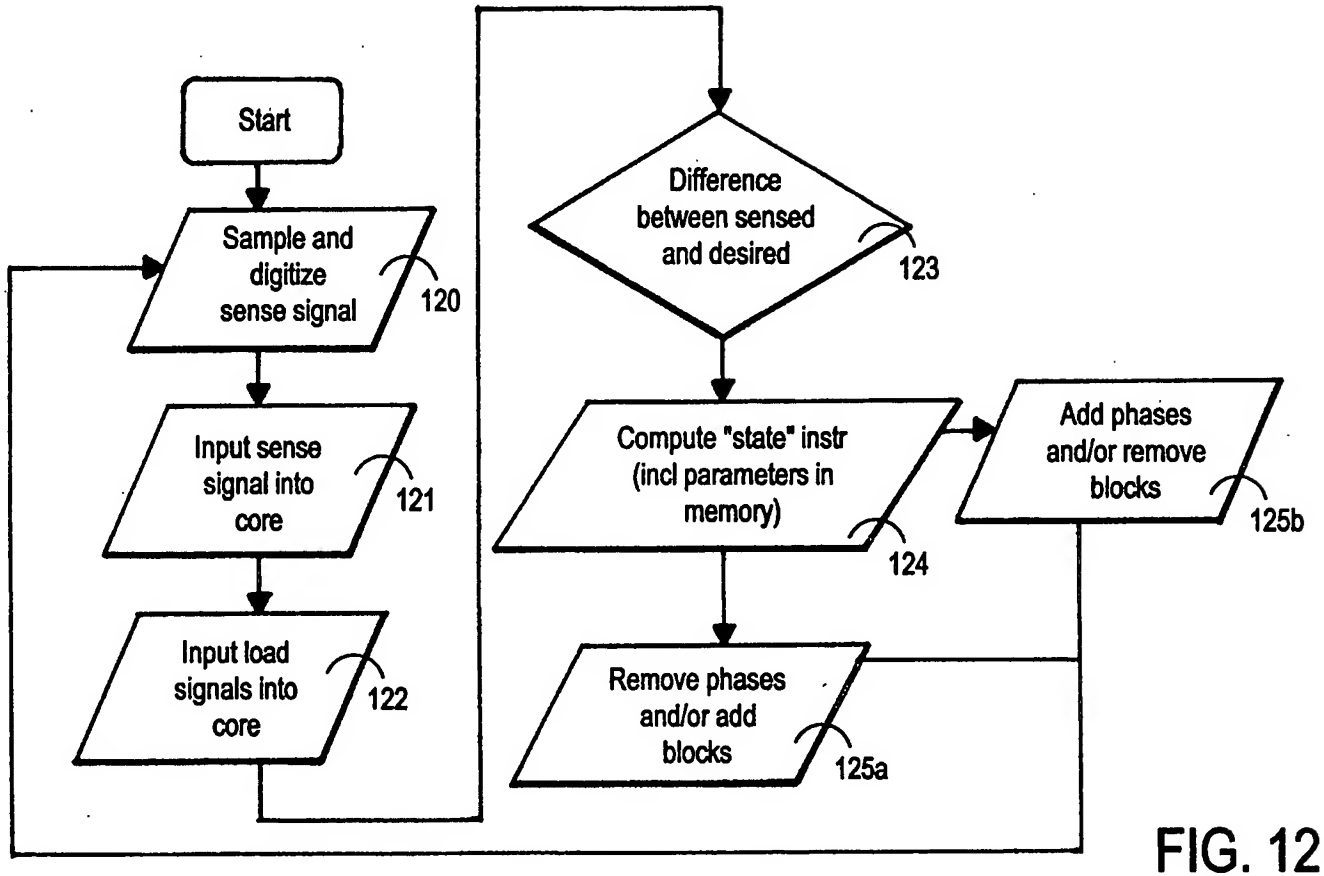

Start
Sample and digitize sense signal
120
Input sense signal into core
121
Input load signals into core
122
Difference between sensed and desired
123
Compute "state" instr (incl parameters in memory)
124
Add phases and/or remove blocks
125b
Remove phases and/or add blocks
125a

FIG. 12

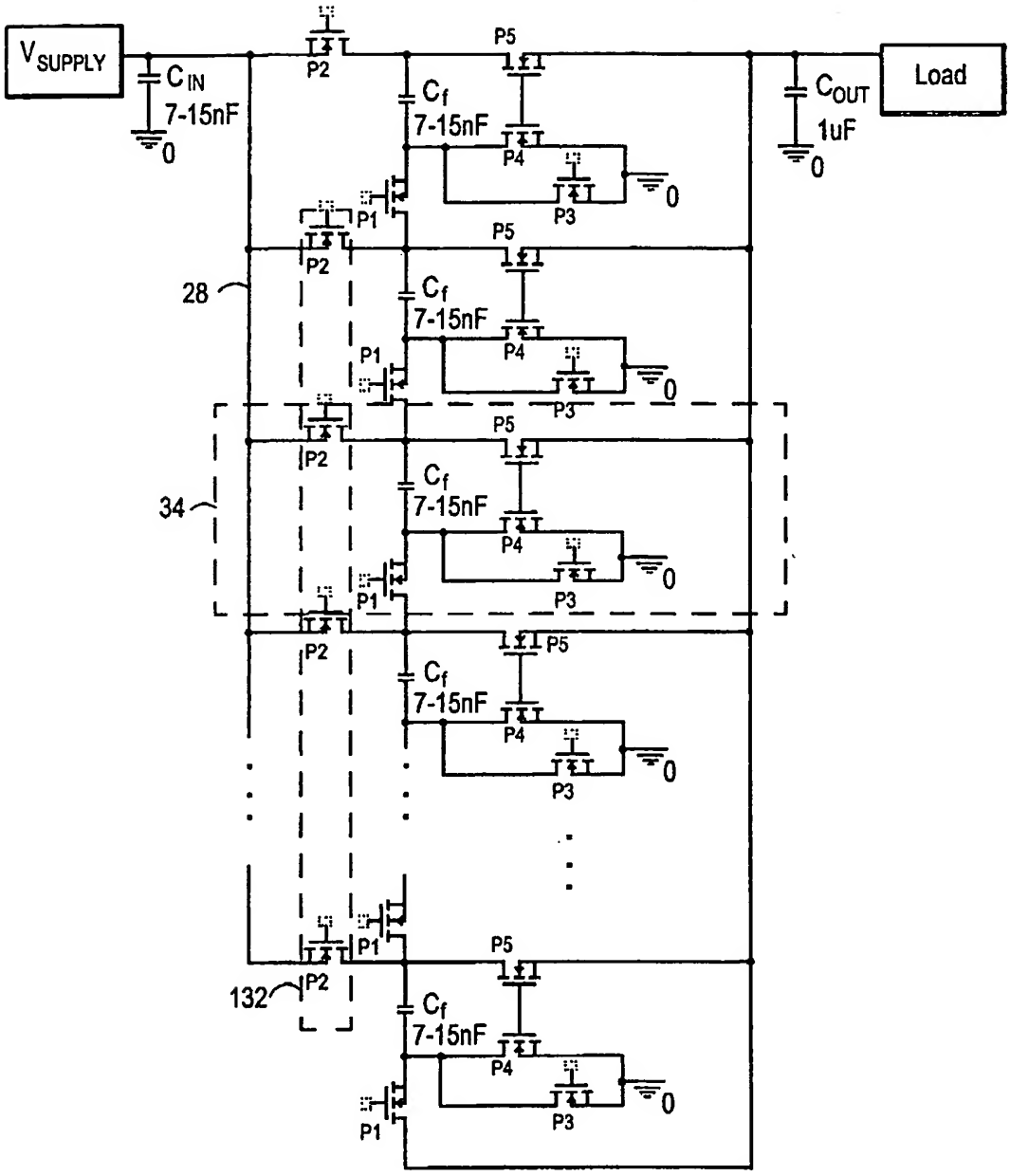

V SUPPLY
C IN
7-15nF
0
P2
P5
C f
7-15nF
P4
P3
P1
C OUT
1uF
Load
28
34
132

FIG. 13

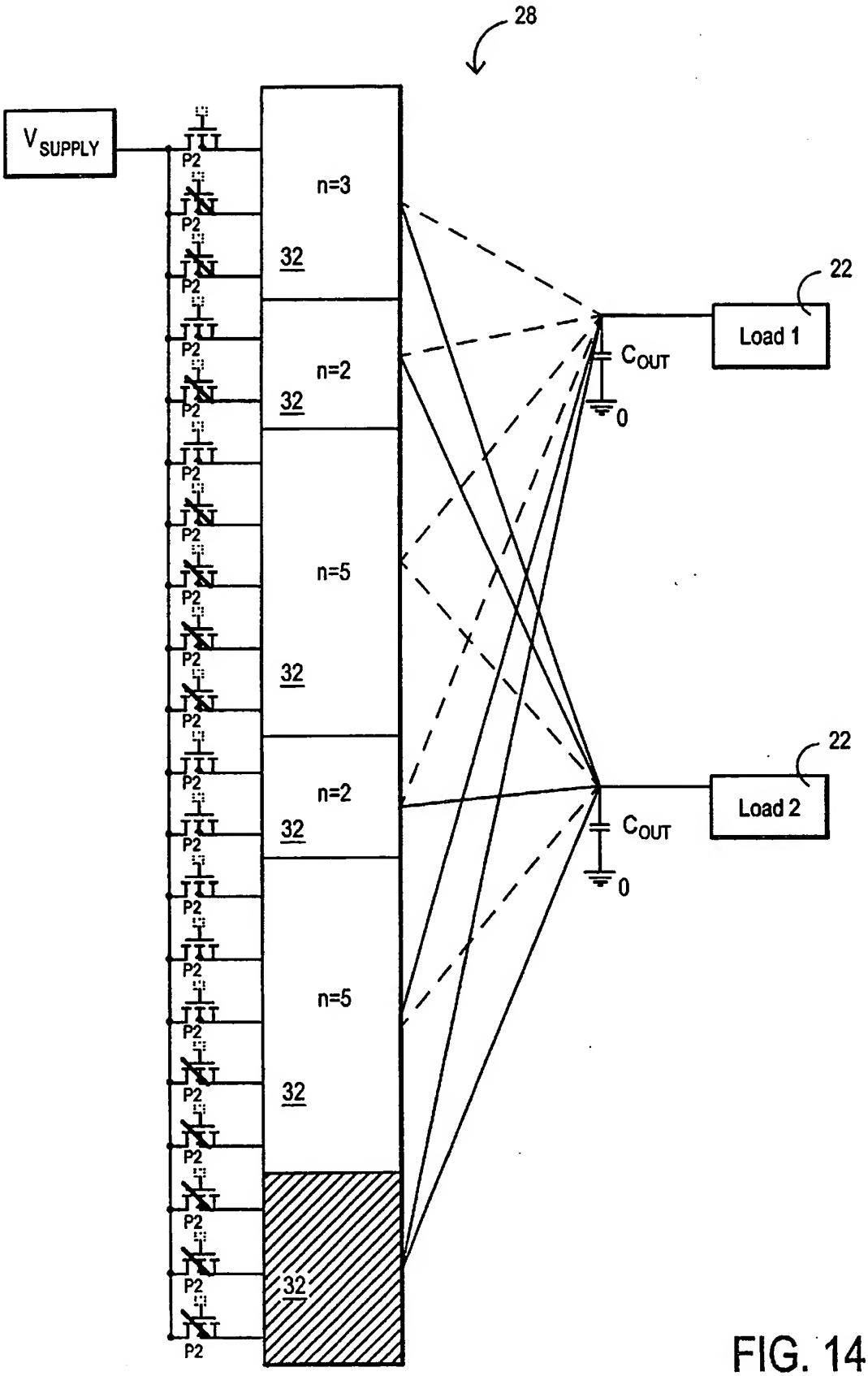

28
V_{SUPPLY}
P2
n=3
32
n=2
32
n=5
32
n=2
32
n=5
32
32
22
Load 1
C_{OUT}
0
22
Load 2
C_{OUT}
0

FIG. 14

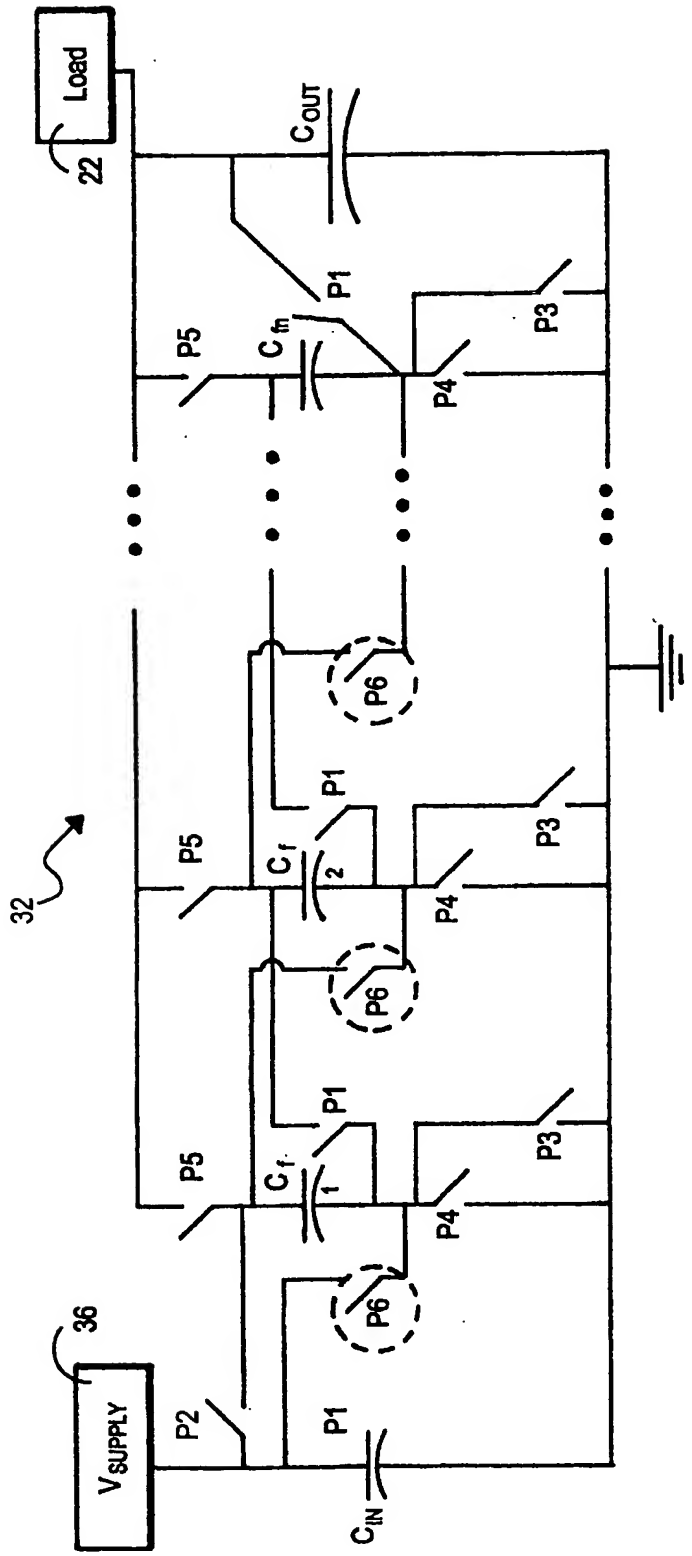


FIG. 15

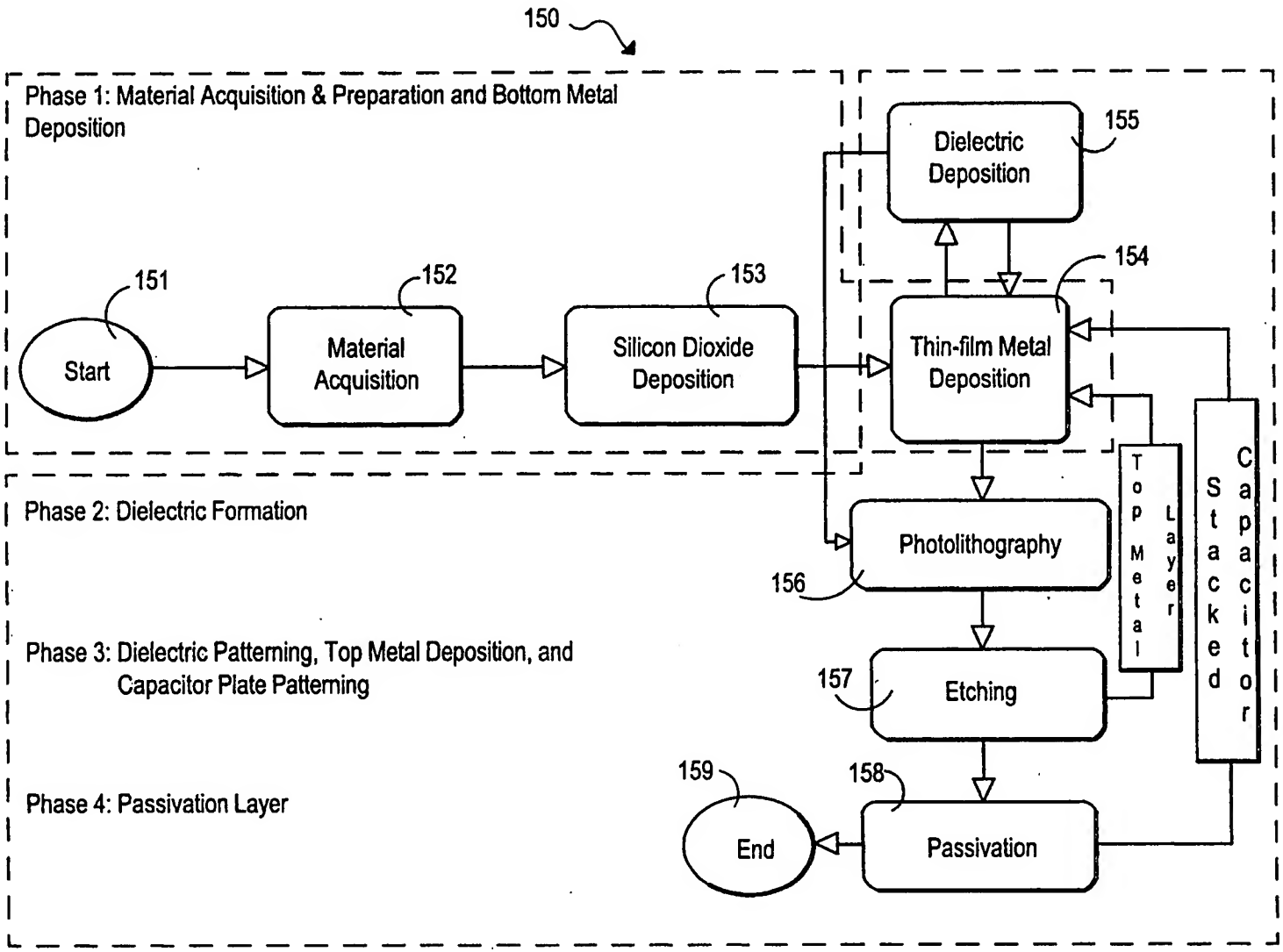

150
Phase 1: Material Acquisition & Preparation and Bottom Metal Deposition
Start
151
Material Acquisition
152
Silicon Dioxide Deposition
153
Dielectric Deposition
155
Thin-film Metal Deposition
154
Phase 2: Dielectric Formation
Photolithography
156
Top Metal Layer
Stacked Capacitor
Phase 3: Dielectric Patterning, Top Metal Deposition, and Capacitor Plate Patterning
Etching
157
Phase 4: Passivation Layer
End
159
Passivation
158

FIG. 16

PHASE	PROCESS STEPS		DESCRIPTION/NOTES
	MATERIAL ACQUISITION & PREPARATION		
	Obtain Silicon Wafer	1	Standard 8" Silicon (6"for prototype)
1	Deposit SiO2	2	0.5-1.0 µm (insulation and adhesion)
	BOTTOM METAL DEPOSITION		
	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	Deposit Tantalum	3	2000 Å
	DIELECTRIC FORMATION		
2	Tantalum Oxide Deposition	1	*Anodization*
	DIELECTRIC PATTERNING		MASK 1
	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Tantalum Oxide	4	Typically RIE
	Etch Tantalum	5	Typically RIE
	TOP METAL DEPOSITION		
3	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	TOP METAL PATTERNING		MASK 2
	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Copper	4	Wet or dry
	Etch Titanium	5	Wet or dry
	Strip Resist	6	
	PASSIVATION (OPTIONAL)		
	Apply BCB	1	
4	Exposure	2	
	Develop	3	
	Cure	4	

FIG. 17

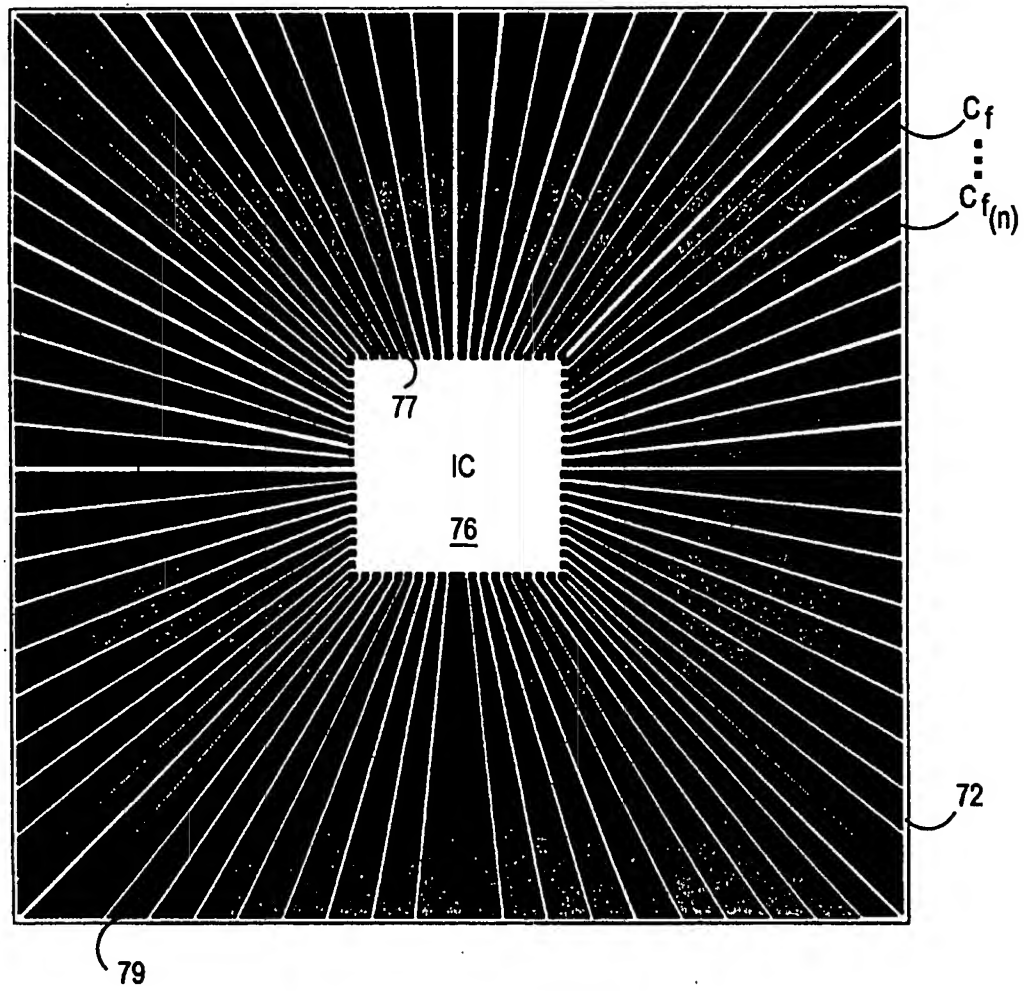


FIG. 18

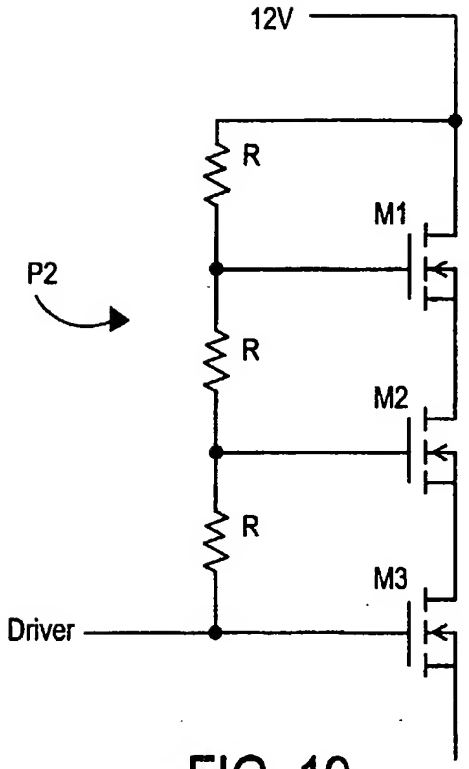


FIG. 19

Input Voltage	Gate Length (Process)	Qg(pC)	Fsw(MHz)
12	0.8 um	>40	1-5
12	0.5 um	27	10-20
5	0.5 um	27	10-20
5	0.35 um	20	20-30
3.3	0.35 um	20	20-30
3.3	0.25 um	10	50-60
3.3	0.18 um	6	80-100

FIG. 20

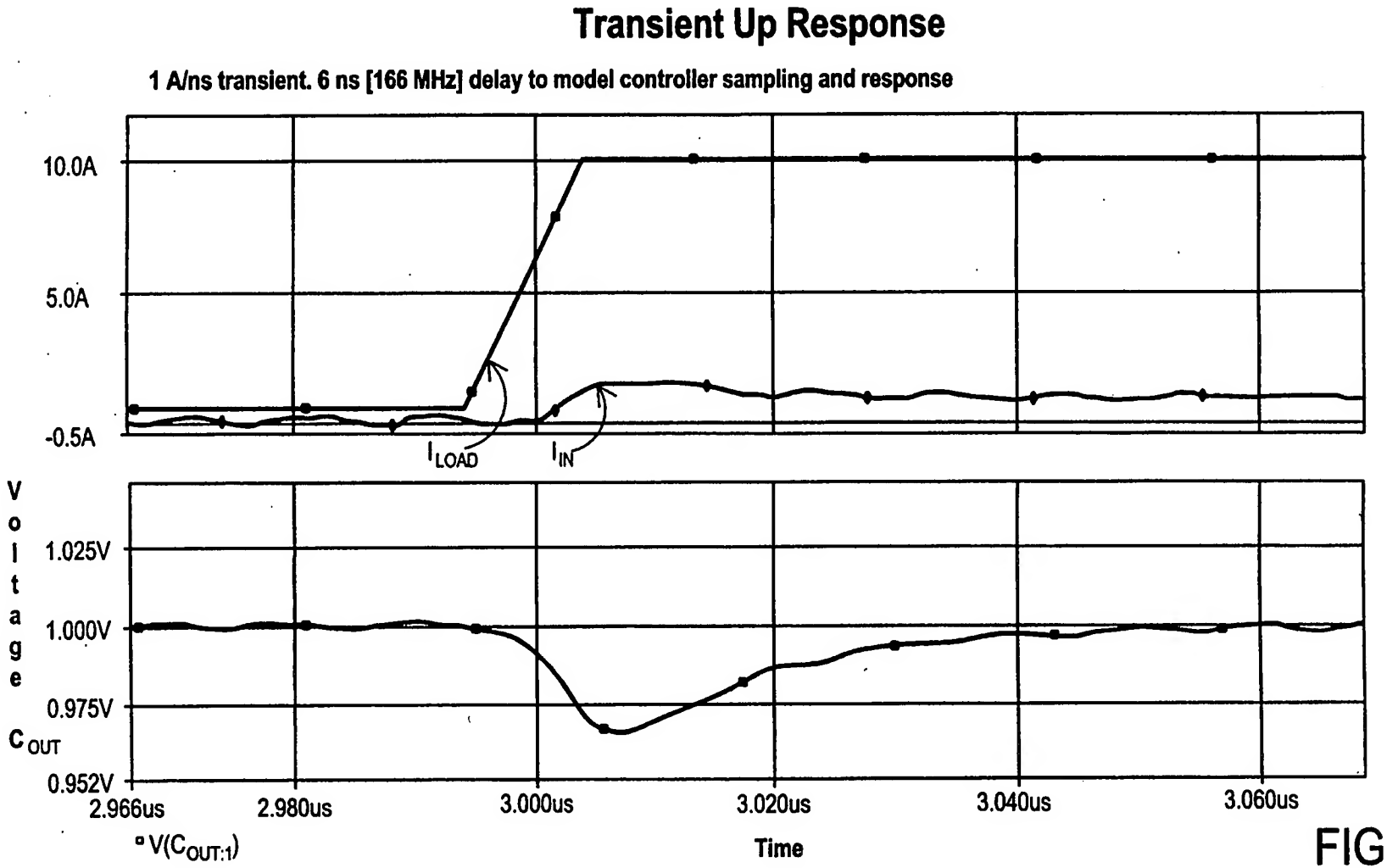

Transient Up Response
1 A/ns transient. 6 ns [166 MHz] delay to model controller sampling and response
10.0A
5.0A
-0.5A
I_{LOAD}
I_{IN}
Voltage
1.025V
1.000V
0.975V
C_{OUT}
0.952V
2.966us
2.980us
3.000us
3.020us
3.040us
3.060us
V($C_{OUT:1}$)
Time

FIG. 21

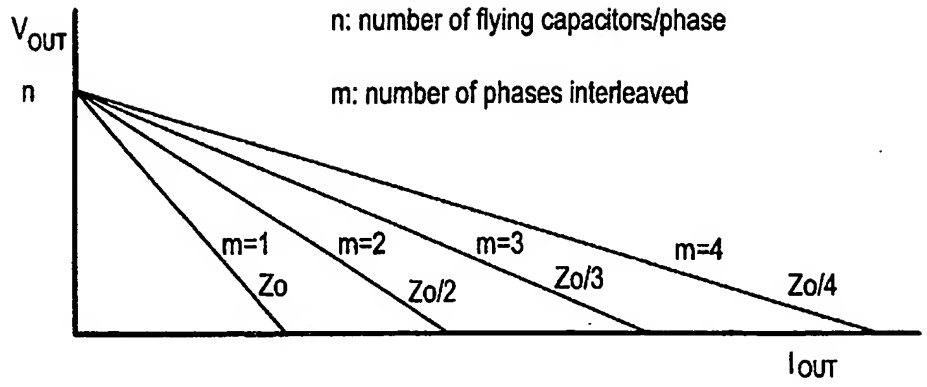

V_{OUT}
n
n: number of flying capacitors/phase
m: number of phases interleaved
m=1
Zo
m=2
Zo/2
m=3
Zo/3
m=4
Zo/4
I_{OUT}

FIG. 22

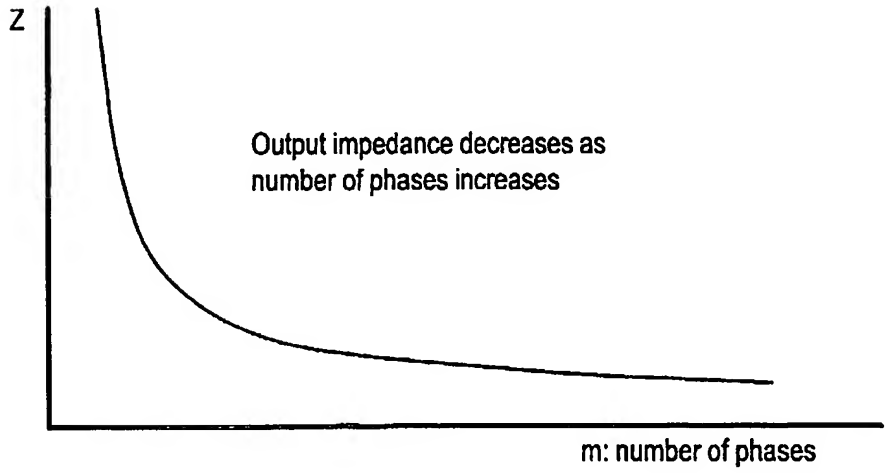

Z
Output impedance decreases as
number of phases increases
m: number of phases

FIG. 23

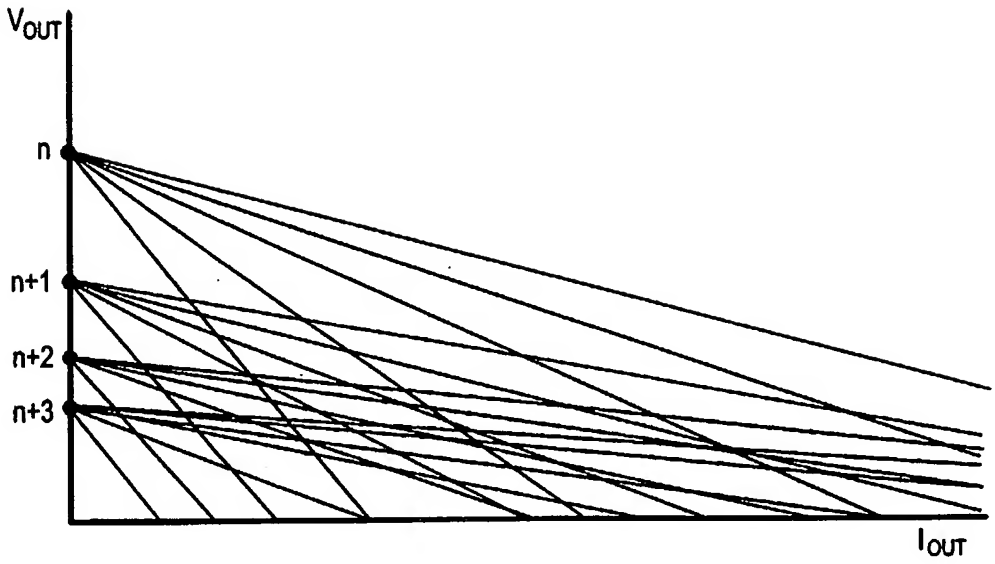

V_{OUT}
n
n+1
n+2
n+3
I_{OUT}

FIG. 24

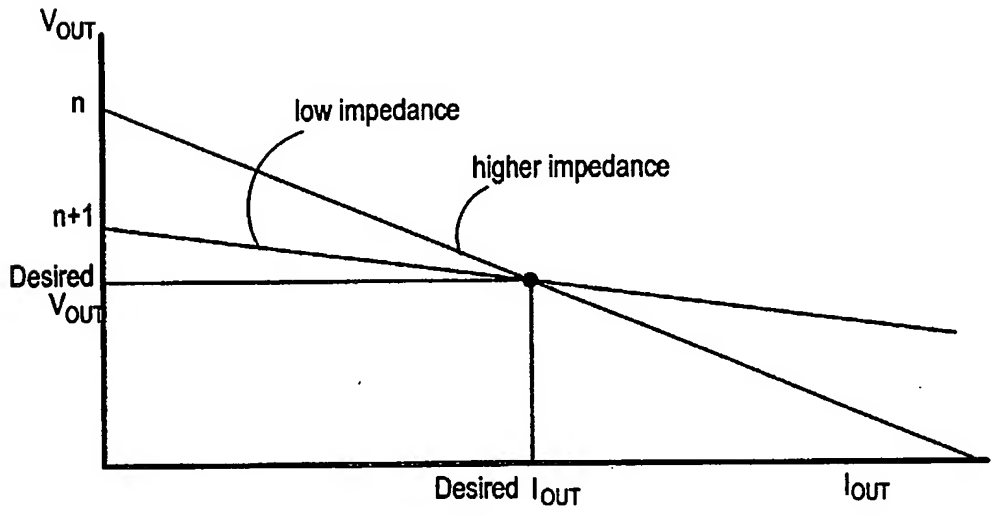

V_{OUT}
n
low impedance
higher impedance
n+1
Desired
V_{OUT}
Desired I_{OUT}
I_{OUT}

FIG. 25

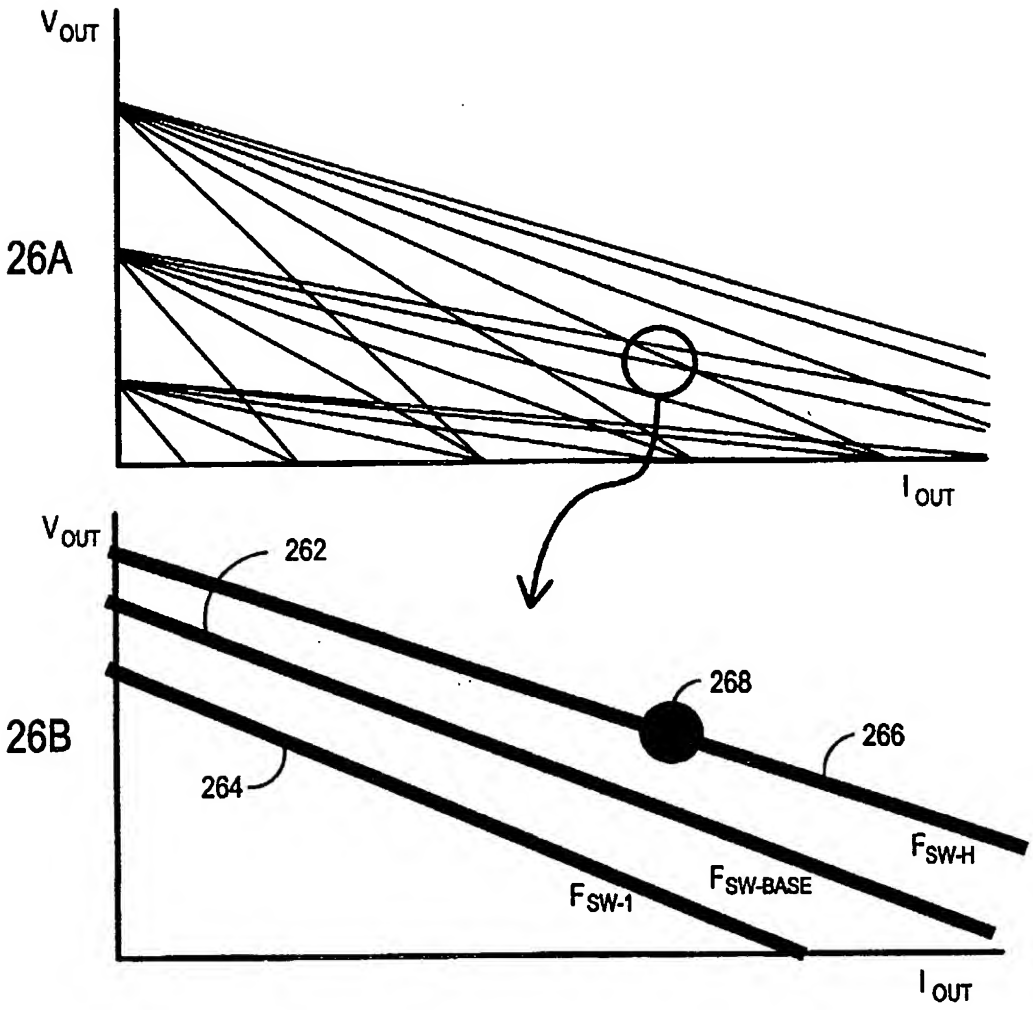


FIG. 26

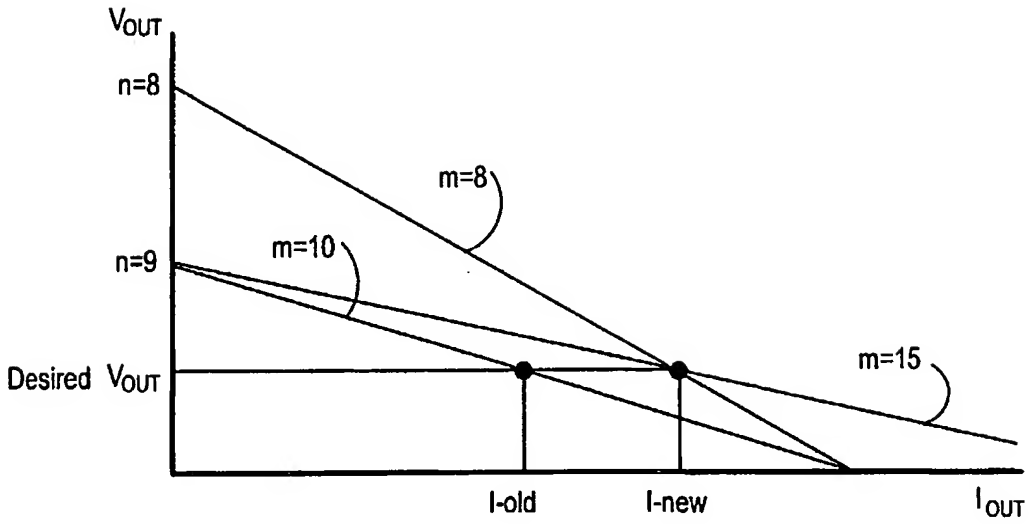

V_{OUT}
n=8
m=8
n=9
m=10
Desired V_{OUT}
m=15
I-old
I-new
I_{OUT}

FIG. 27

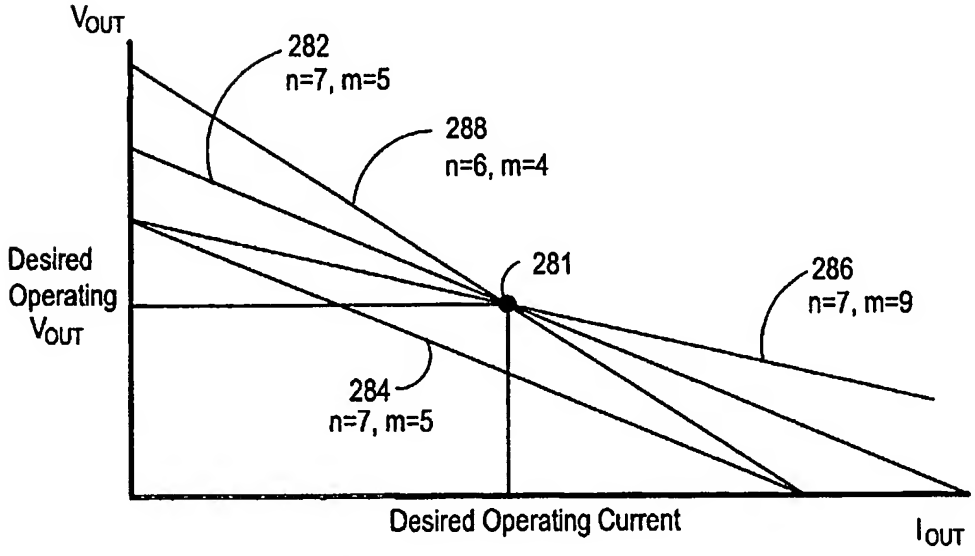

V_{OUT}
282
n=7, m=5
288
n=6, m=4
Desired
Operating
V_{OUT}
281
286
n=7, m=9
284
n=7, m=5
Desired Operating Current
I_{OUT}

FIG. 28

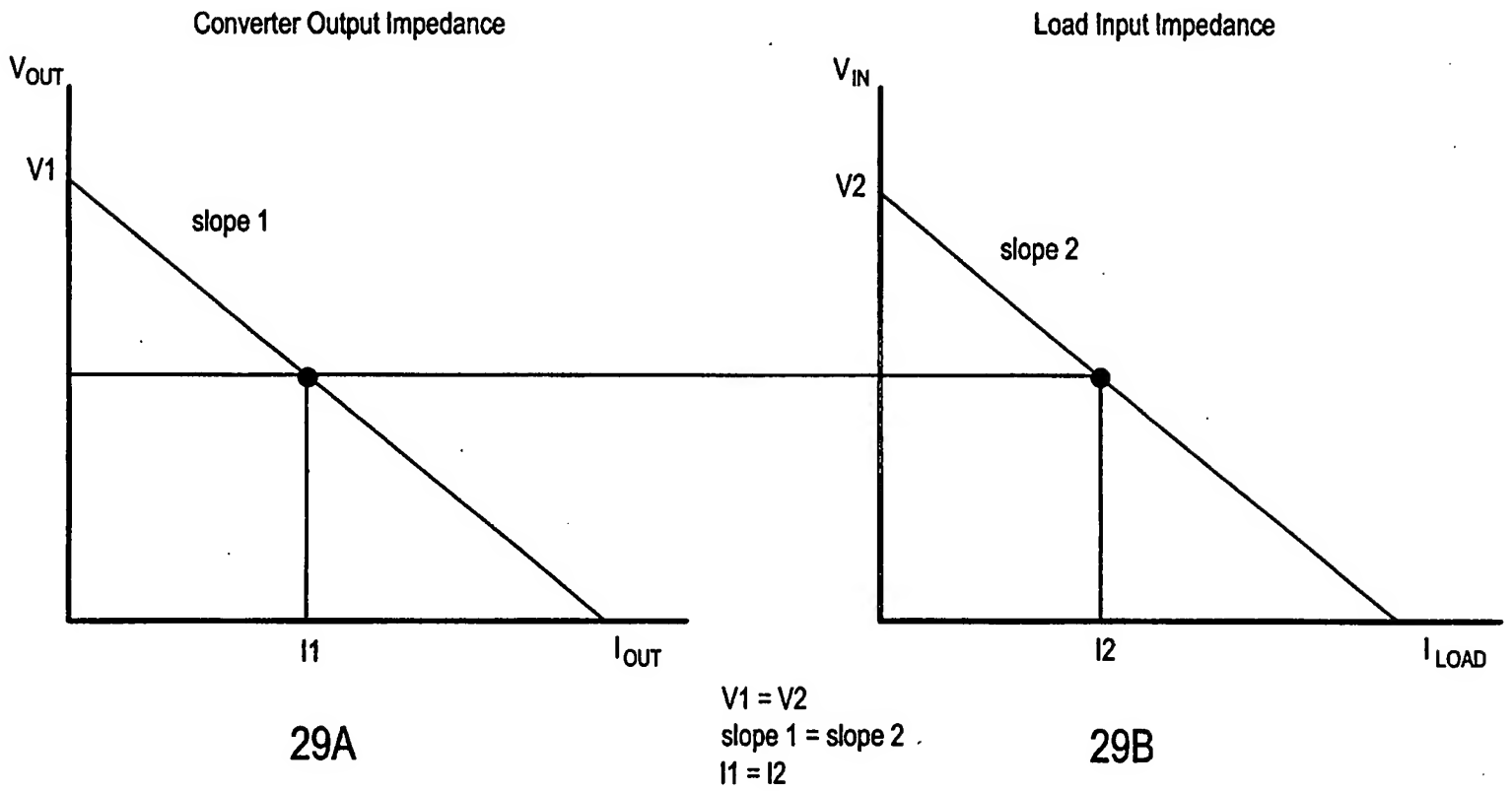
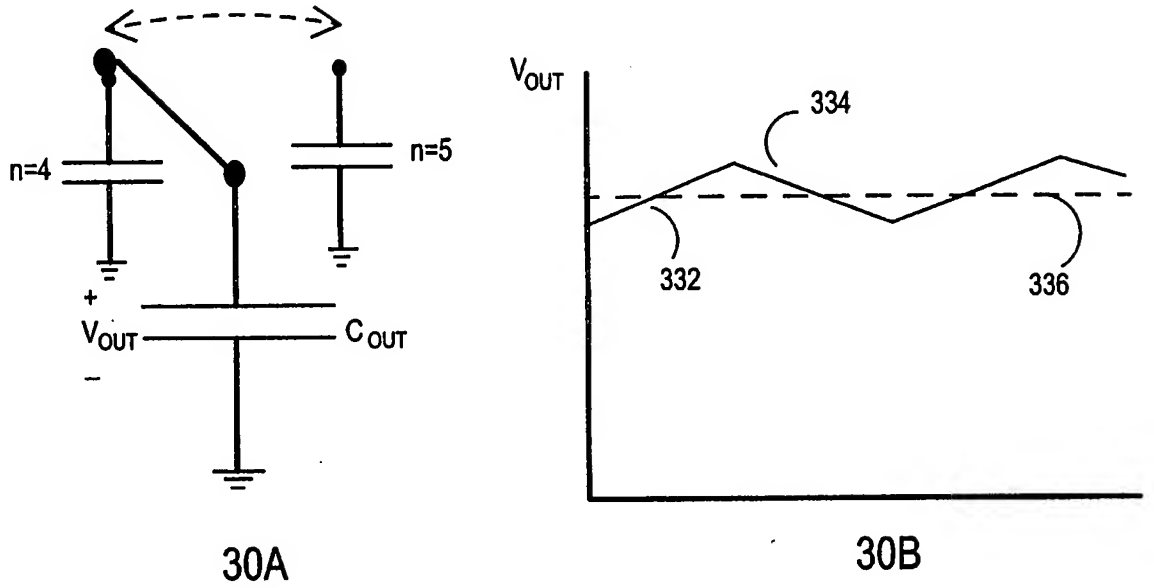
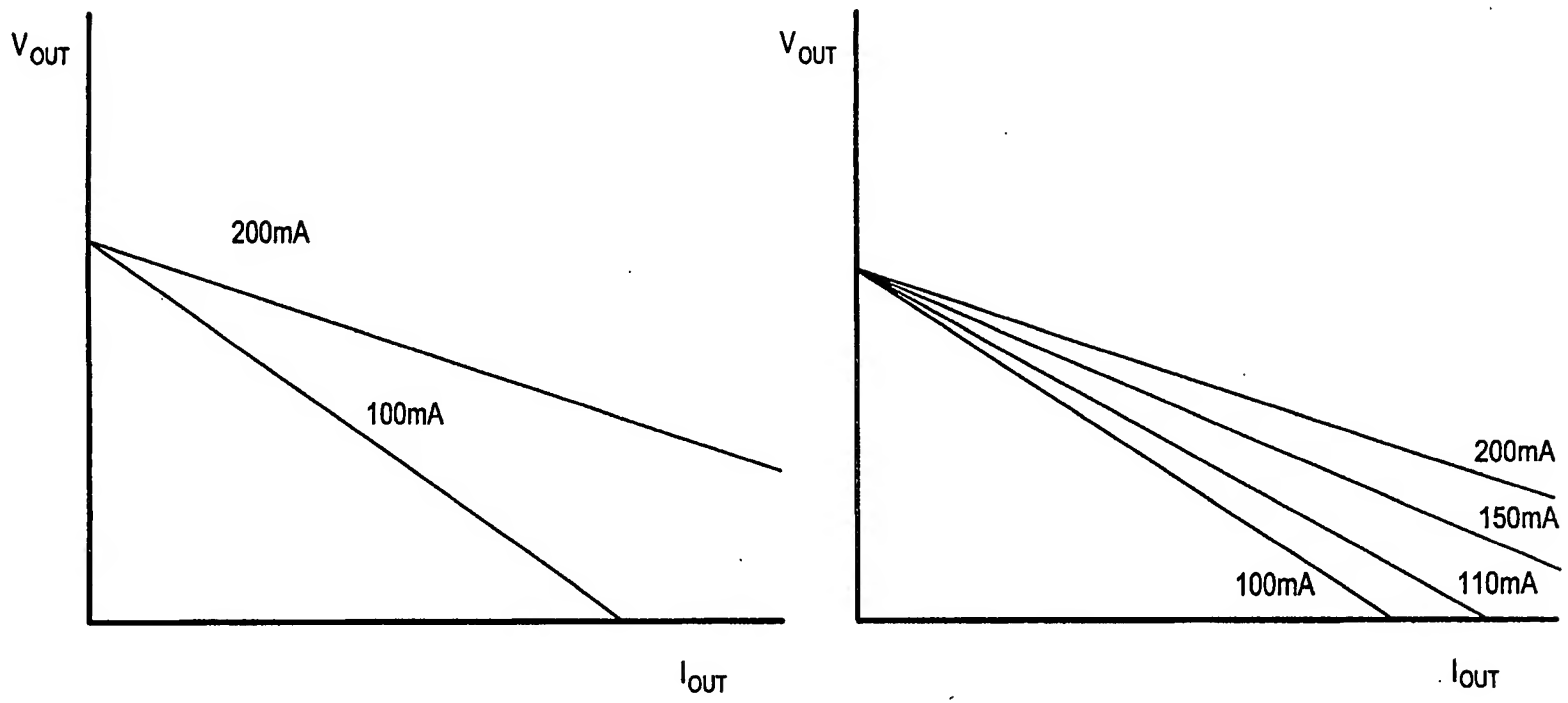

Converter Output Impedance
V_{OUT}
V1
slope 1
I1
I_{OUT}
29A
Load Input Impedance
V_{IN}
V2
slope 2
I2
I_{LOAD}
29B
V1 = V2
slope 1 = slope 2
I1 = I2

FIG. 29



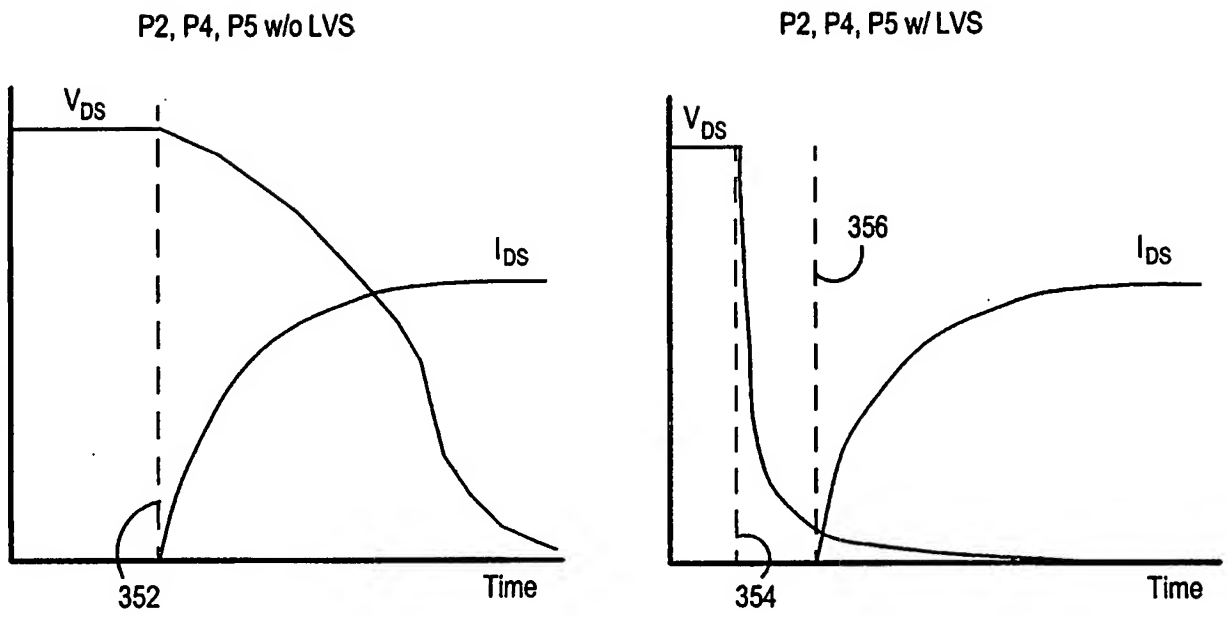
30A 30B

FIG. 30



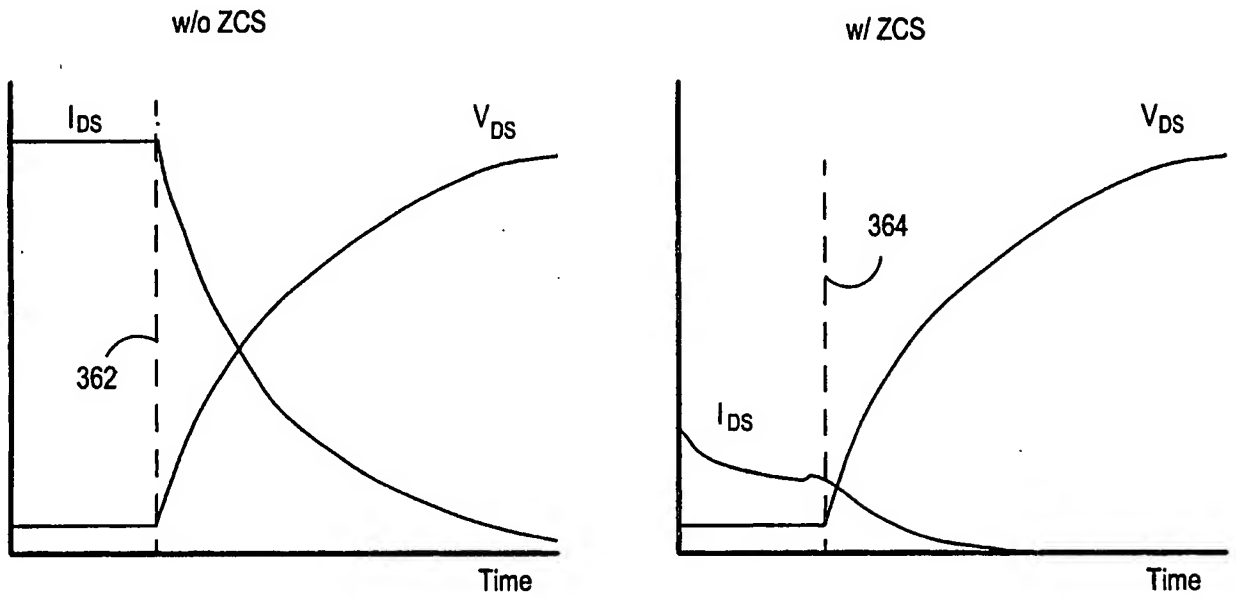
31A 31B

FIG. 31



32A 32B

FIG. 32



33A 33B

FIG. 33

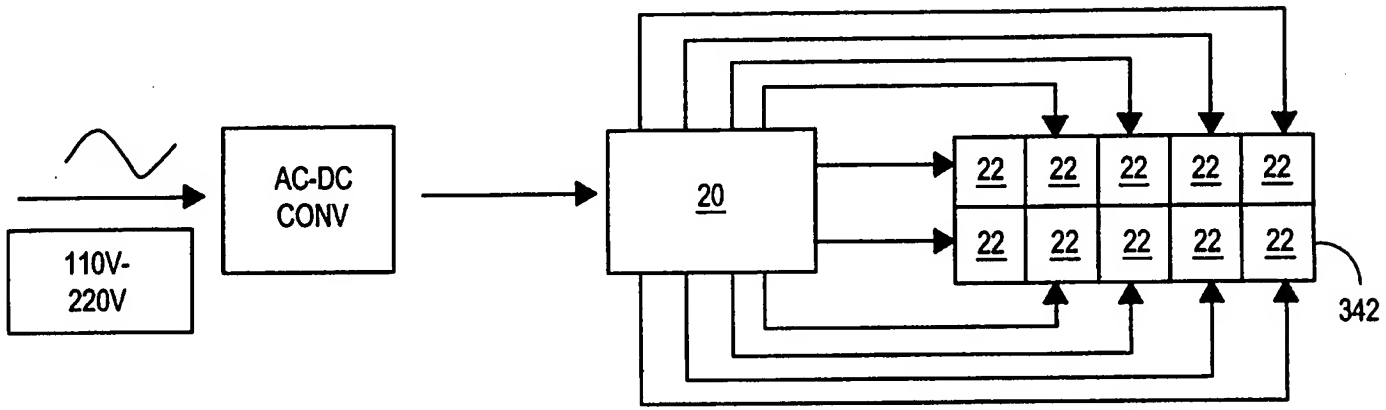

AC-DC
CONV
110V-
220V
20
22
22
22
22
22
22
22
22
22
22
342

FIG. 34

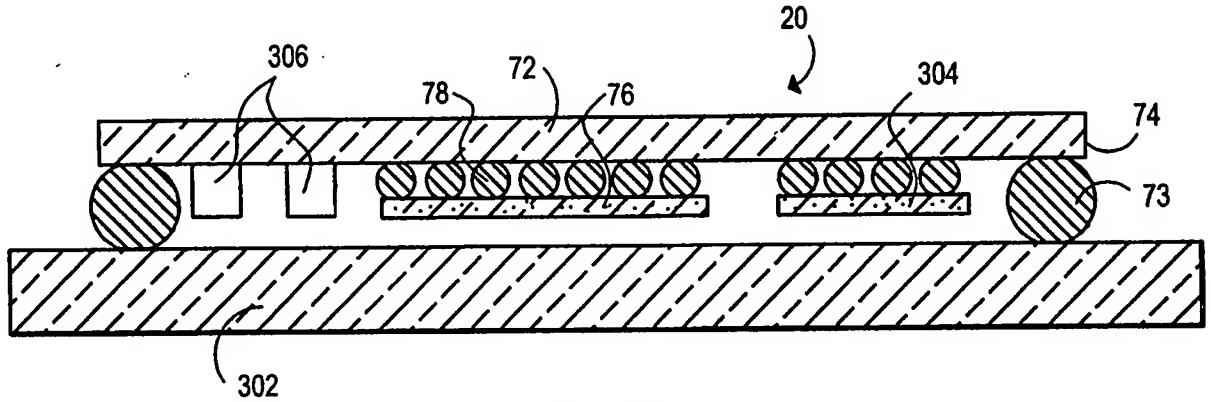

20
306
72
78
76
304
74
73
302

FIG. 35

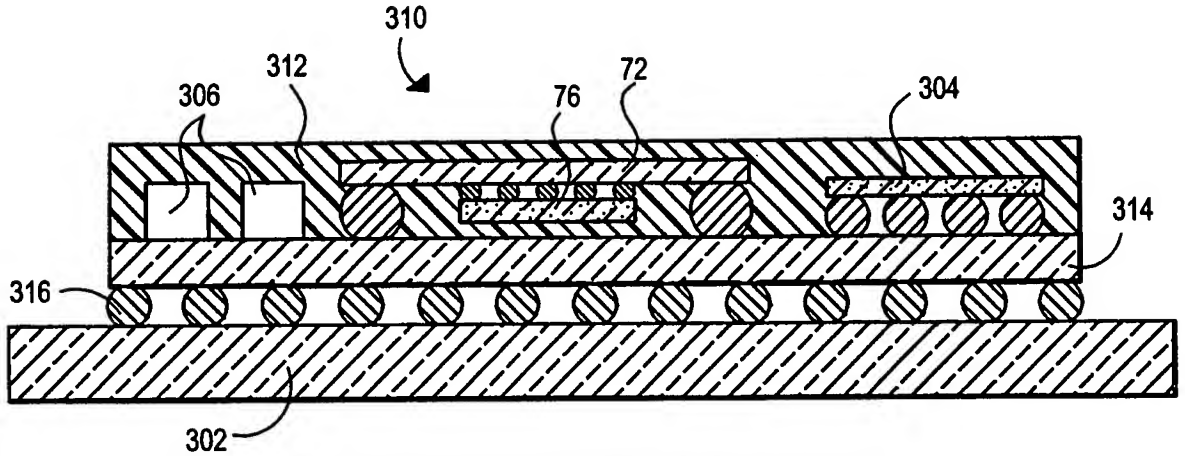

310
312
306
76
72
304
314
316
302

FIG. 36

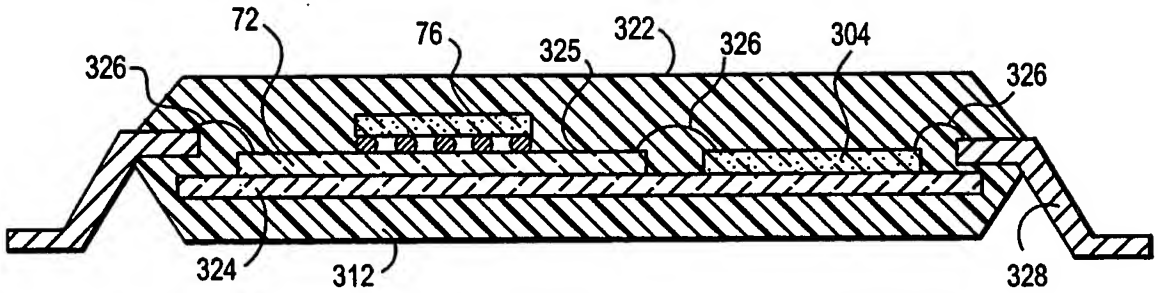

72
76
325
322
326
304
326
326
324
312
328

FIG. 37

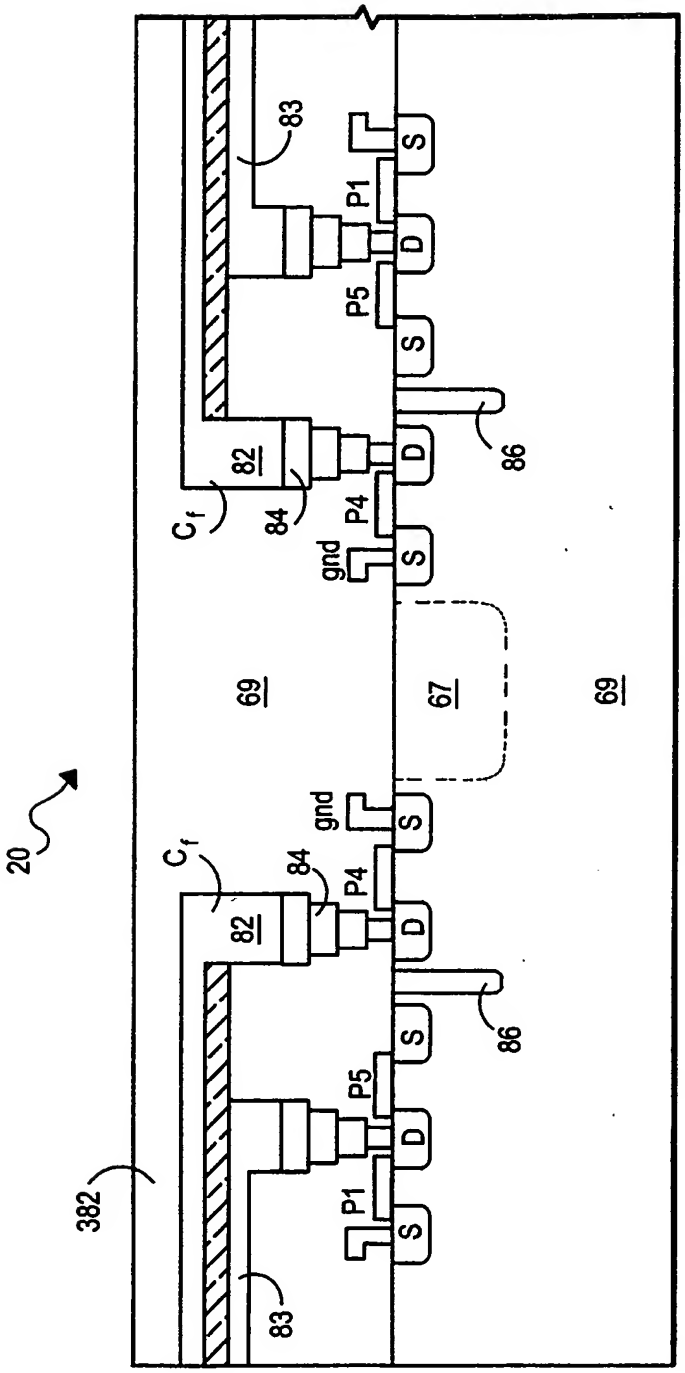

20
382
83
P1
S
D
P5
S
86
82
84
C_f
P4
gnd
S
69
67
69
gnd
S
C_f
84
P4
82
D
S
86
P5
D
P1
S
83

FIG. 38